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What Is Claimed Is:

1. A semiconductor substrate having a given horizontal cross-section, a first region defined in a first portion of the given horizontal cross-section of the substrate, and a second region defined in a second portion of the given horizontal cross-section of the substrate, the second region adjacent to and integral with the first region, a first given plurality of quantum wells formed in the first region, the first given plurality of quantum wells having a first given bandgap, and a second given plurality of quantum wells formed in the second region, the second given plurality of quantum wells having a second given bandgap, wherein the first given bandgap is less than the second given bandgap.

2. A semiconductor substrate according to claim 1 further comprising a third region defined in a third portion of the given horizontal cross-section of the substrate, the third region adjacent to and integral with the second region, a third given plurality of

quantum wells formed in the third region, and the third given plurality of quantum wells having a third given bandgap, wherein the third given bandgap is less than the second given bandgap.

3. A semiconductor structure comprising:

a semiconductor substrate having a given horizontal cross-section, a first section defined in one portion of the given horizontal cross-section of the substrate, and a second section defined in another portion of the given horizontal cross-section of the substrate;

a first plurality of quantum wells formed in the first section, the first plurality of quantum wells having a given bandgap;

a second plurality of quantum wells formed in the second section, the second plurality of quantum wells modified by depositing a dielectric cap on the second section, and rapid thermal annealing of the dielectric cap for a given time and at a given temperature, so as to tune the second plurality of quantum wells to a tuned bandgap;

wherein the tuned bandgap is greater than the given bandgap.

4. A semiconductor substrate according to claim 3 wherein the dielectric cap comprises SiO_2.

5. A semiconductor substrate according to claim 3 wherein the dielectric cap comprises TiO_2.

6. A semiconductor substrate according to claim 3 wherein the dielectric cap comprises Si_3N_4.

7. A semiconductor substrate according to claim 3 wherein the dielectric cap comprises Ta_2O_5.

8. A semiconductor substrate according to claim 3 wherein the dielectric cap comprises B, P doped glass.

9. A semiconductor substrate according to claim 3 wherein the dielectric cap is deposited on the second section by electron beam sputtering.

10. A semiconductor substrate according to claim 3 wherein the dielectric cap is deposited on the second section by ion beam sputtering.

11. A semiconductor substrate according to claim 3 wherein the given temperature is above 650^0 C.

12. A semiconductor substrate according to claim 3 wherein the given temperature comprises a range of about 650^0 C to about 900^0 C.

13. A semiconductor substrate according to claim 3 wherein a sacrificial layer is positioned on the second section prior to depositing the dielectric cap on the second section.

14. A semiconductor substrate according to claim 13 wherein the sacrificial layer is graded from a first portion at a first height to a second portion at a second height, and further wherein the first height is lower than the second height.

15. A semiconductor substrate according to claim 13 wherein the sacrificial layer is stepped from a first substantially flat portion to a second substantially flat portion, and further wherein the first substantially flat portion is lower than the second substantially flat portion.

16. A semiconductor substrate according to claim 13 wherein the sacrificial layer on the second section comprises a given portion of the single semiconductor wafer designated as the sacrificial layer.

17. A semiconductor substrate according to claim 13 wherein the sacrificial layer positioned on the second section comprises a dielectric layer deposited thereon.

18. A semiconductor substrate according to claim 13 wherein the sacrificial layer positioned on the second section comprises a metal layer deposited thereon.

19. A semiconductor substrate according to claim 3 wherein a sacrificial top cladding layer is deposited on the second section prior to depositing a dielectric cap.

20. A semiconductor substrate according to claim 19 wherein the sacrificial top cladding layer comprises a stepped top surface.

21. A semiconductor substrate according to claim 19 wherein the sacrificial top cladding layer comprises an inclined top surface.

22. A semiconductor substrate according to claim 19 wherein the sacrificial top cladding layer is deposited by a gray scale masking technique.

23. A semiconductor substrate according to claim 19 wherein the sacrificial top cladding layer is deposited by a dry etching technique.

24. A semiconductor substrate according to claim 3 wherein ion implantation is provided to the second section.

25. A semiconductor substrate according to claim 24 wherein the ion implantation introduces into the second section at least one selected from a group consisting of impurities and vacancies.

26. A semiconductor substrate according to claim 25 wherein the selected at least one of impurities and vacancies are introduced into the second section at a first given height in a first area and at a second given height in a second area.

27. A semiconductor substrate according to claim 26 wherein an implantation mask is deposited on the top surface of the second section so as to introduce the at least one of impurities and vacancies at the first given height and the second given height in the first area and the second area, respectively.

28. A semiconductor substrate according to claim 3 wherein at least one of the first section and the second section are individually excited so as to tune output light through the semiconductor substrate.

29. A semiconductor substrate according to claim 3 wherein the semiconductor substrate is a single wafer comprising multiple laser sources formed by the first section and the second section, respectively.

30. A semiconductor substrate comprising:

a single semiconductor wafer having a first end and a second end in opposition to one another, and a longitudinal axis formed between the first end and the second end;

a plurality of quantum wells formed in the single semiconductor wafer between the first end and the second end, a first section of the plurality of quantum wells having a first given bandgap, and a second section of the plurality of quantum wells having a second given bandgap;

wherein the second given bandgap is greater than the first given bandgap.

31. A semiconductor substrate according to claim 30 wherein the plurality of quantum wells are configured to have an increasing bandgap shift in a given direction parallel to the longitudinal axis from the first portion to the second portion.

32. A semiconductor substrate according to claim 31 wherein the increasing bandgap shift of the plurality of quantum wells is a substantially smooth increase in the given direction parallel to the longitudinal axis.

33. A semiconductor substrate according to claim 31 wherein the increasing bandgap shift of the plurality of quantum wells from the first section to the second section comprises at least one given length of a substantially constant bandgap shift.

34. A semiconductor substrate according to claim 33 wherein the increasing bandgap shift comprises a stepwise increase in the given direction parallel to the longitudinal axis.

35. A semiconductor substrate according to claim 33 wherein the plurality of quantum wells are configured in at least two regions, and further wherein each of the at least two regions have a substantially constant bandgap in the given direction parallel to the longitudinal axis, respectively.

36. A method for forming a semiconductor substrate, the method comprising:

providing a single semiconductor wafer having a first end and a second end in opposition to one another, a longitudinal axis formed between the first end and the second end, a top surface and a bottom surface in opposition to one another, a plurality of quantum wells disposed in the semiconductor wafer, and the plurality of quantum wells having a given bandgap;

depositing a first dielectric cap on a first given portion of the top surface of the single semiconductor wafer; and

rapid thermal annealing of the first dielectric cap deposited on the top surface of the single semiconductor material to tune the plurality of quantum wells disposed beneath the first dielectric cap from the given bandgap to a first tuned bandgap;

wherein the first tuned bandgap is greater than the given bandgap.

37. A method according to claim 36 wherein the top surface of the single semiconductor is entirely covered by the first given portion.

38. A method according to claim 37 further comprising the steps of depositing a second dielectric cap on the top surface of the single semiconductor wafer subsequent to the step of rapid thermal annealing of the first dielectric cap, the second dielectric cap configured to cover a second given portion of the top surface of the single semiconductor

wafer, the second given portion having a smaller surface area than the first given portion, and rapid thermal annealing of the second dielectric cap deposited on the top surface of the single semiconductor material to further tune the plurality of quantum wells disposed beneath the second dielectric cap from the first tuned bandgap to a second tuned bandgap, wherein the second tuned bandgap is greater than the first tuned bandgap.

39. A method according to claim 38 further comprising the steps of depositing a third dielectric cap on the top surface of the single semiconductor wafer subsequent to the step of rapid thermal annealing of the second dielectric cap, the third dielectric cap configured to cover a third given portion of the top surface of the single semiconductor wafer, the third given portion configured within the second given portion, the third given portion having a smaller surface area than the second given portion, and rapid thermal annealing of the third dielectric cap deposited on the top surface of the single

semiconductor material to further tune the plurality of quantum walls disposed beneath the third dielectric cap from the second tuned bandgap to a third tuned bandgap, wherein the third tuned bandgap is greater than the second tuned bandgap.

40. A method according to claim 39 wherein the single semiconductor wafer comprises a first section, a second section, and a third section, the first section consisting of the plurality of quantum wells disposed beneath the first portion exclusive of the second portion, the second section consisting of the plurality of quantum wells disposed beneath the second portion exclusive of the third portion, and the third section consisting of the plurality of quantum wells disposed beneath the third portion, wherein the first section has the first tuned bandgap, the second section has the second tuned bandgap, and the third section has the third tuned bandgap.

41. A method according to claim 40 wherein the first section has a first given photoluminescence

shift corresponding to the first tuned bandgap, the second section has a second given photoluminescence shift corresponding to the second tuned bandgap, and the third section has a third given photoluminescence shift corresponding to the third tuned bandgap.

42. A method according to claim 36 wherein the top surface of the single semiconductor wafer is partially covered by the first given portion so as to provide a given uncapped portion.

43. A method according to claim 42 further comprising the steps of depositing a second dielectric cap on the top surface of the single semiconductor wafer subsequent to the step of rapid thermal annealing of the second dielectric cap, the second dielectric cap configured to cover a second given portion of the top surface of the single semiconductor wafer, the second given portion configured within the first given portion, the second given portion having a smaller surface area than the first given portion, and rapid thermal annealing of the second dielectric cap

deposited on the top surface of the single semiconductor material to further tune the plurality of quantum walls disposed beneath the second dielectric cap from the first tuned bandgap to a second tuned bandgap, wherein the second tuned bandgap is greater than the first tuned bandgap.

44. A method according to claim 43 further comprising the steps of depositing a third dielectric cap on the top surface of the single semiconductor wafer subsequent to the step of rapid thermal annealing of the second dielectric cap, the third dielectric cap configured to cover a third given portion of the top surface of the single semiconductor wafer, the third given portion configured within the second given portion, the third given portion having a smaller surface area than the second given portion, and rapid thermal annealing of the third dielectric cap deposited on the top surface of the single semiconductor material to further tune the plurality of quantum walls disposed beneath the third dielectric cap from the second tuned bandgap to a third tuned

bandgap, wherein the third tuned bandgap is greater than the second tuned bandgap.

45. A method according to claim 44 wherein the single semiconductor wafer comprises a first section, a second section, a third section, and a fourth section, the first section consisting of the plurality of quantum wells disposed beneath the given uncapped portion, the second section consisting of the plurality of quantum wells disposed beneath the first portion exclusive of the second portion, the third section consisting of the plurality of quantum wells disposed beneath the second portion exclusive of the third portion, and the fourth section consisting of the plurality of quantum wells disposed beneath the third portion, wherein the first section comprises the given bandgap, the second section comprises the first tuned bandgap, the third section comprises the second tuned bandgap, and the fourth section comprises the third tuned bandgap.

46. A method according to claim 45 wherein the first section has a first given photoluminescence shift corresponding to the given bandgap, the second section has a second given photoluminescence shift corresponding to the first tuned bandgap, the third section has a third given photoluminescence shift corresponding to the second tuned bandgap, and the fourth section has a fourth given photoluminescence shift corresponding to the third tuned bandgap.

47. A method according to claim 36 wherein the first dielectric cap deposited on the first given portion has a first given region and a second given region, the first given region having a first given height and the second given area having a second given height, the first given height being lower than the second given height, wherein the step of rapid thermal annealing of the first dielectric cap tunes the plurality of quantum cells disposed beneath the first given area to a first tuned bandgap and the plurality of quantum wells disposed beneath the second given

area to a second tuned bandgap, and wherein the second tuned bandgap is greater than the first tuned bandgap.

48. A method according to claim 47 wherein the top surface of the single semiconductor wafer is entirely covered by the first given portion.

49. A method according to claim 47 wherein the top surface of the single semiconductor wafer is partially covered by the first given portion so as to provide a given uncapped portion.

50. A method according to claim 36 wherein the first dielectric cap deposited on the first given portion has a first given area, a second given area, and a third given area, the first given area having a first given height, the second given area having a second given height, and the third given area having a third given height, the first given height being lower than the second given height, and the second given height being lower than the third given height, wherein the step of rapid thermal annealing of the

first dielectric cap tunes the plurality of quantum wells beneath the first given area to a first tuned bandgap, the plurality of quantum wells beneath the second given area to a second tuned bandgap, and the plurality of quantum wells beneath the third given area to a third tuned bandgap, wherein the third tuned bandgap is greater than the second tuned bandgap, and the second tuned bandgap is greater than the first tuned bandgap.

51. A method according to claim 50 wherein the top surface of the single semiconductor wafer is entirely covered by the first given portion.

52. A method according to claim 50 wherein the top surface of the single semiconductor wafer is partially covered by the first given portion so as to provide a given uncapped portion.

53. A method according to claim 52 wherein the single semiconductor wafer comprises a first section, a second section, a third section, and a fourth

section, the first section consisting of the plurality of quantum wells disposed beneath the given uncapped portion, the second section consisting of the plurality of quantum wells disposed beneath the first given region, the third section consisting of the plurality of quantum wells disposed beneath the second given region, and the fourth section consisting of the plurality of quantum wells disposed beneath the third given region, wherein the first section comprises the given bandgap, the second section comprises the first tuned bandgap, the third section comprises the second tuned bandgap, and the fourth section comprises the third tuned bandgap.

54. A method according to claim 53 wherein the first section comprises a first given photoluminescence shift corresponding to the given bandgap, the second section comprises a second given photoluminescence shift corresponding to the first tuned bandgap, the third section comprises a photoluminescence shift corresponding to the second tuned bandgap, and the fourth section comprises a

fourth given photo luminescence shift corresponding to the third tuned bandgap.

55. A method according to claim 36 wherein the first dielectric cap comprises SiO_2.

56. A method according to claim 36 wherein the step of depositing the first dielectric cap on the first given portion of the top surface of the single semiconductor wafer comprises electron beam sputtering.

57. A method according to claim 36 wherein the step of depositing the first dielectric cap on the first given portion of the top surface of the single semiconductor wafer comprises ion beam sputtering.

58. A method according to claim 57 wherein the first section comprises a first given photoluminescence shift corresponding to the given bandgap, the second section comprises a second given photoluminescence shift corresponding to the first

tuned bandgap, the third section comprises a photoluminescence shift corresponding to the second tuned bandgap, and the fourth section comprises a fourth given photoluminescence shift corresponding to the third tuned bandgap.

59. A method according to claim 58 wherein at least one of the first section, the second section, the third section, and the fourth section are individually excited so as to tune output light.

60. A method according to claim 58 wherein the single semiconductor wafer further comprises multiple laser sources formed by the first section, the second section, the third section, and the fourth section, respectively.

61. A method according to claim 36 wherein the first dielectric cap comprises SiO_2.

62. A method according to claim 36 wherein the step of depositing the first dielectric cap on the

first given portion of the top surface of the single semiconductor wafer comprises electron beam sputtering.

63. A method according to claim 36 wherein the step of depositing the first dielectric cap on the first given portion of the top surface of the single semiconductor wafer comprises ion beam sputtering.

64. A method according to claim 36 wherein the step of rapid thermal annealing is subjected to the single semiconductor wafer for a given time.

65. The method of claim 36 wherein the step of rapid thermal annealing is subjected to the semiconductor wafer at a given temperature.

66. The semiconductor substrate according to claim 65 wherein the given temperature is above 650^{o} C.

67. The method of claim 65 wherein the given temperature comprises a range of about 650° C to 900° C.

68. A method according to claim 36 further comprising the step of positioning a sacrificial layer on the single semiconductor wafer prior to the step of depositing the first dielectric cap on the top surface of the single semiconductor wafer.

69. A method according to claim 68 wherein the sacrificial layer is graded from a first portion at a first height to a second portion at a second height, the first height being lower than the second height.

70. A method according to claim 68 wherein the sacrificial layer is stepped from a first substantially flat portion to a second substantially flat portion, and further wherein the first substantially flat portion is lower than the second substantially flat portion.

71. A method according to claim 68 wherein the sacrificial layer on the single semiconductor wafer comprises a given portion of the single semiconductor wafer designated as the sacrificial layer.

72. A method according to claim 68 wherein the sacrificial layer positioned on the single semiconductor wafer comprises a dielectric layer deposited thereon.

73. A method according to claim 68 wherein the sacrificial layer positioned on the single semiconductor layer comprises a metal layer deposited thereon.

74. A method according to claim 36 further comprising the step of depositing a sacrificial top cladding layer on the top surface of the single semiconductor wafer prior to the step of depositing a first dielectric cap.

75. A method according to claim 74 wherein the sacrificial top cladding layer comprises a stepped top surface.

76. A method according to claim 74 wherein the sacrificial top cladding layer comprises an inclined top surface.

77. A method according to claim 74 wherein the sacrificial top cladding layer is deposited by a gray scale masking technique.

78. A method according to claim 74 wherein the sacrificial top cladding layer is deposited by a dry etching technique.

79. A method according to claim 36 further comprising a step of providing ion implantation to the top surface of the single semiconductor wafer.

80. A method according to claim 79 wherein the ion implantation introduces into the single

semiconductor wafer at least one selected from a group consisting of impurities and vacancies.

81. A method according to claim 80 wherein the selected at least one of impurities and vacancies are introduced into the single semiconductor at a first given height in a first section and at a second given height in a second section.

82. A method according to claim 81 further comprising the step of depositing an implantation mask on the top surface of the single semiconductor wafer so as to introduce the at least one of impurities and vacancies at the first given height and the second given height in the first section and the second section, respectively.

83. A semiconductor structure comprising:

a semiconductor substrate having a given horizontal cross-section, a first section defined in one portion of the given horizontal cross-section of the substrate, and a second section defined in another

portion of the given horizontal cross-section of the substrate;

a first plurality of quantum wells formed in the first section, the first plurality of quantum wells having a given bandgap;

a second plurality of quantum wells formed in the second section, the second plurality of quantum wells modified by depositing a cap on the second section, and rapid thermal annealing of the cap for a given time and at a given temperature, so as to tune the second plurality of quantum wells to a tuned bandgap;

wherein the tuned bandgap is greater than the given bandgap.

84. A method for forming a semiconductor substrate, the method comprising:

providing a single semiconductor wafer having a first end and a second end in opposition to one another, a longitudinal axis formed between the first end and the second end, a top surface and a bottom surface in opposition to one another, a plurality of

quantum wells disposed in the semiconductor wafer, and the plurality of quantum wells having a given bandgap;

depositing a first cap on a first given portion of the top surface of the single semiconductor wafer; and

rapid thermal annealing of the first cap deposited on the top surface of the single semiconductor material to tune the plurality of quantum wells disposed beneath the first cap from the given bandgap to a first tuned bandgap;

wherein the first tuned bandgap is greater than the given bandgap.